Patent Claims

1. Method for producing transistor structures with LDD, in which

a gate electrode (3) is structured on a gate dielectric (2), on an essentially planar upper surface of a semiconductor body or substrate (1), and

using the gate electrode (3) as a mask, implantations of dopant are performed for the purpose of creating source/drain regions (12) and regions (11) of lower dopant concentration that are adjacent to the former on the channel side,

characterized in that

after the structuring of the gate electrode (3) the substrate (1) is etched such that on the source side and on the drain side sloping sidewalls (5) are formed adjacent to the gate electrode (3) and sloping downward toward the outside from the gate electrode (3),

a spacer layer (6) is deposited, conforming with the edges, which is then anisotropically back-etched to form spacers (7), which at least partially cover the source-side and drain-side sidewalls of the gate electrode (3) and the sloping sidewalls (5), and the implantation of dopant is performed at a high angle relative to the original upper surface of the substrate to form the source and drain regions (12) and at a low angle relative to the original upper surface of the substrate, through the spacers (7), to form the regions (11) of lower dopant concentration.

2. Method according to claim 1, in which

the sloping sidewalls (5) are formed at a slope angle of 30° to 60° from the original upper surface of the substrate (1).

3. Method according to claim 2, in which

the sloping sidewalls (5) are formed at a slope angle of 45° from the original upper surface of the substrate (1).

4. Method according to one of claims 1 through 3, in which the implantation for the purpose of forming the regions (11) of lower dopant concentration is performed in a direction that, in an intersecting plane that is oriented vertically on the upper surface of the substrate (1) and the sloping sidewalls (5), forms an angle of between 30° and 60° with a surface normal on the original upper surface of the substrate (1).

5. Method according to one of claims 1 through 4, in which the implantation for the purpose of forming the source and drain regions (12) is performed in a direction that, in an intersecting plane that is oriented vertically on the upper surface of the substrate (1) and the sloping sidewalls (5), forms an angle of between 0° and 7° with a surface normal on the original upper surface of the substrate (1).

6. Method according to one of claims 1 through 5, in which, in the etching of the sloping sidewalls (5), the substrate (1) is also etched away somewhat underneath the gate electrode (3).

7. Method according to one of claims 1 through 6, in which with the etching of the sloping sidewalls (5) the upper surface of the substrate (1) is lowered by a depth (d), which ranges from 20 nm to 200 nm.